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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/636,143	08/06/2003	Bruc Rosenthal	AME-004	2812
22888	7590	02/06/2007	EXAMINER	
BEVER HOFFMAN & HARMS, LLP			SHINGLETON, MICHAEL B	
TRI-VALLEY OFFICE			ART UNIT	PAPER NUMBER
1432 CONCANNON BLVD., BLDG. G				
LIVERMORE, CA 94550			2817	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/06/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)
	10/636,143	ROSENTHAL, BRUCE
	Examiner	Art Unit
	Michael B. Shingleton	2817

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on _____.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-23 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner. Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a). Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.

- 4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) Notice of Informal Patent Application
- 6) Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

Claims 1-23 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for the pulling of the voltage on the output terminal to a value near the voltage provided by a voltage the specification, does not reasonably provide enablement for an invention that pulls the voltage on the output terminal “to” the voltage provided by a voltage source such as the “first voltage source” as termed in some of the claims. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make the invention commensurate in scope with these claims. The invention disclosed in the specification is one where a transistor of the source follower 505 is connected in parallel with another transistor 507 of opposite conductivity type that provides a lower impedance from the output terminal to the voltage source as compared to having just one of the transistors turned on. However, this arrangement can never actually pull the voltage on the output terminal “to” the voltage provided by the voltage source because the “another transistor” will always have some sort of impedance drop across the source and drain terminals. From applicant’s specification this pulling of the voltage can approach the voltage of the source but never achieve it and the language of the claims requires that it actually reach this voltage. Accordingly, the examiner’s position is supported by applicant’s own specification. Note page 8 where the p-channel transistor is recited as “almost a perfect switch” but it is not a perfect switch as admitted by applicant and applicant has taught how to make a “perfect switch” that would enable the pulling of the voltage on the output terminal “to” the voltage provided by a voltage source. The claims do not adequately recite how close the output voltage will be to the voltage source. Now, the examiner will read the claims for examining purposes not as if the voltage on the output terminal is actually pulled to the voltage provided by the voltage source but is pulled to some other voltage that maybe close to the voltage source. In particular the following rejection(s) involving Dowlatabadi US 6,271,699 below utilizes a p-channel transistor like transistor 37 connected in parallel with the source follower 36 and therefore since transistor 37 when “on” has the same impedance as that of applicant’s disclosed invention this prior art will be read as pulling the output terminal voltage “to” the voltage source voltage even though the prior art can not do this but neither can applicant’s disclosed invention. Similarly, the current source like 506 of the instant invention just can not pull the voltage on the output terminal to the voltage VDDA in the embodiment that is described in the specification because there will be some impedance in the current source. Applicant just has not taught how to make a perfect current source. In fact the examiner does not see any specific examples of current source construction. Accordingly, any voltage that a current source pulls the output voltage to will be

read as pulling the voltage on the output to the voltage of the voltage source like VDDA. The examiner must give such a broad reading to the claims as the actual range of values is not specifically recited. Again the claim while being specific to reciting that voltage source and the output voltage are equal, this cannot be and the claims do not recite how close the output voltage is actually to the supply voltage. When reading the specification the examiner does not see any specific mentioning of exactly what this range is. For example the output voltage is to be within one percent of the total supply voltage.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6, 8-13, and 15-22 in so far as understood are rejected under 35 U.S.C. 102(b) as being anticipated by Dowlatabadi US 6,271,699 (Dowlatabdi).

(Note that the following rejection attempts to follow the exact wording of a set of specific claims so that applicant can readily set how the claimed subject matter is met by the prior art. For example the claim set based on independent claim 1 is basically used here, and there maybe some terminologies from other claim sets specifically used in this rejection when the examiner feels that the specific mentioning of these terminologies is needed. Even though other claims employs different wording for the same subject matter than is specifically mentioned in this rejection, the subject matter being rejected is never-the-less clear. Repeating the exact wording of every claim set would not result in a clear and concise office action. The examiner makes every effort to form a clear and concise office action by also pointing to the various elements and passages to help applicant see how the claimed invention is met by the prior art. Applicant should also note that if a limitation is not specifically recited in great detail in this office action that this does not mean that the prior art does not have such a feature. Features that are so self-evidence may not be recited in great detail for this would not result in a clear and concise office action, but would cloud the subject matter that is the most important to the invention. The reference to the prior art and the specific Figures of the prior should be sufficient to show this subject matter and the Office action refers to this. The subject matter that is most important to the invention would be like for example, the use of a p-

channel transistor connected in parallel with the n-channel transistor so as to further the voltage to a point closer to the voltage of the voltage source which seems to be paramount to this invention. (See page 8, around line 12 of the instant application.) Figure 1 and the relevant text of Dowlatabdi disclose a source follower circuit having an input terminal like " V_{REF} " and an output terminal " V_{OUT} ". The source follower has a first device "36" wherein the first device has n-channel conductive properties like that of transistor 505 of the disclosed invention. It is self-evident that the first device 36 of Dowlatabdi is coupled between the first voltage source " V_{DD} " and a second voltage source " V_{SS} ". The element 38 of Dowlatabdi does form a "current source coupled to the second voltage source". Applicant is referred to the passages of Dowlatabdi that include column 4, around lines 44-54, Figure 2 that shows the activation of the p-channel device that is as applicant says "almost a perfect switch" and the pulling of the voltage of the output terminal to be very close to the " V_{DD} " voltage, column 6, around lines 25-39 that recites the functional subject matter of the claims. If the "first device" 36 of Dowlatabdi is not conducting then the current source 38 for this source follower arrangement is "on" and will accordingly pull the voltage on the output to value that is close to the second voltage source voltage " V_{SS} ". When the "first device" 36 is conducting at the full level then the output voltage will be the voltage " V_{DD} " minus the threshold voltage of the first device (See Figure 2 of Dowlatabdi.). Note that this is self-evident because of the n-channel transistor of Dowlatabdi being the same as the n-channel 505 of the instant invention, but note that column 6 around line 25 of Dowlatabdi mentioned above describes this threshold voltage effect. The functional language that requires the "second device" 37 to have "second conducting properties" that are different from the first conductive properties is as also self-evident because the second device 37 is a p-channel whereas the first device is an n-channel. This appears to be the paramount feature of the instant invention that enables the pulling of the voltage of the voltage on the output terminal "to the voltage provided by the first voltage source". While this rejection is a 35 USC 102 rejection, it is noted in order to help applicant that the teaching of Dowlatabdi of providing of this addition switching device could be used in other source follower circuits and the motivation to do so would be to approach the actual rail voltage as much as possible. The claimed functional language requires no furthering limiting structure, but note that the "second device" 37 receives a different input signal than the first device 37 as is clearly evident in Figure 1 of Dowlatabdi. Note that the gate or sometimes called the control terminal of the second device 37 of Dowlatabdi is connected to the output of the device 28 of Dowlatabdi. This is not the same input signal as is applied to the control terminal of the first device 36 of Dowlatabdi. The subject matter that is represented by at least claim 2 is addressed above and in particular note the column 6 passage discussed above. The subject matter that is represented by at least claim 3 is already clearly

addressed above. Note the conductivity types of the first and second devices mentioned above. The subject matter that is represented by at least claim 4 is broad for what is a "low voltage" and a "high voltage" source? Thus the examiner has given a broad interpretation to this subject matter and has found that the one could call the " V_{DD} " voltage a "low voltage" and the " V_{SS} " voltage a "high voltage", and vice versa. The subject matter that is represented by at least claim 5 recites the opposite conductivity types that are recited above for the first and second devices. This is to cover the use of an opposite conductivity type circuit that is the same basic circuit structure but uses a positive voltage where a negative voltage was used and a p-channel for an n-channel, etc. However, it happens to be that the invention of Dowlatabdi discloses this opposite arrangement wherein the first device is the p-channel 38, the second device is the n-channel 39 the current source for this first device is the element 36, the first voltage would then be " V_{SS} " and the second voltage would be " V_{DD} ". Likewise the subject matter that is represented by at least claim 6 is as broad as the subject matter represented by at least claim 4. Thus the prior art is seen as anticipating these features.

With respect to the subject matter represented by at least claim 8, applicant is referred to that above as the majority of this subject matter is very specifically mentioned and clearly evidenced. However, the examiner will make it clear that the subject matter that recites a sensing circuit that has the intended use of triggering the second device to conduct when the "amplifier" reaches a saturation point is present in Dowlatabdi for this is met by the element 28 when the first device is a n-channel and is met by the element 29 when the first device is a p-channel. Dowlatabdi does not specifically say "saturation" but the switching is done for the same voltage level as disclosed by the applicant and recited specifically in the above column 6 passage of Dowlatabdi. In fact this subject matter of the exact voltage level point that corresponds to the claimed invention and happens to be the same as that of Dowlatabdi is specifically recited by the subject matter represented by at least claim 9. Thus Dowlatabdi also anticipated the subject matter represented by at least claim 9.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at

the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dowlatabadi US 6,271,699 (Dowlatabadi) in view of Nagel et al. US 4,301,490 (Nagel).

In the interest of clarity and conciseness rather than repeat how the Dowlatabdi reference meets the subject matter that is the base subject matter of these claims rejected in this 103 rejection because of dependency etc., applicant is referred to the above 35 USC 102 rejection involving Dowlatabdi. The subject matter as represented by at least claim 7, recites a "current limiting control circuit" that "disables the first and second devices when the source follower is subjected to abnormal operating conditions". The claims are not specific on what specifically defines "abnormal operating conditions" and nor is the specification, therefore a broad interpretation of this term is given.

Nagel teaches that it is well known to utilize a overload protection circuit with an amplifier so as to protect the amplifier from overload.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have provided the amplifier arrangement of Dowlatabdi with a protection circuit that senses the current and then disables the amplifier so as to protect the amplifier from damage as taught by Nagel.

Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dowlatabdi US 6,271,699 (Dowlatabdi) in view of Sedra et al. "Microelectronic Circuits" (Sedra) and Germano et al. EP 0,446,652A1 (Germano)

In the interest of clarity and conciseness rather than repeat how the Dowlatabdi reference meets the subject matter that is the base subject matter of claim 23 rejected in this 103 rejection applicant is referred to the above 35 USC 102 rejection involving Dowlatabdi. The arrangement of Dowlatabdi lacks a folded cascode. Dowlatabdi is silent on the single ended source that the provides the "V_{IN}" signal. One common source of a single ended signal comes from a folded cascode as shown in Figure 6.45 of Sedra. It is common knowledge that the use of an additional amplifier to provide the input signal to a circuit allows for the signal to have come for a larger distance. To explain this common engineering principle, take for example a cable TV signal. From the signal source the signal is passed through a series of amplifiers that allows the signal source to be located many miles away from the final used or circuit and the use of these amplifiers overcomes the line loss. Telephone systems have the same arrangement. In fact as stated above it is common-place to provide at one in a string of amplifiers to as to allow for the use

of a remote signal. One advantage to the folded cascode as an amplifier is that it avoids the stacking of a large number of transistors across a low voltage power supply as taught by Sedra, i.e. the transistors across a power source the larger the power source has to be in voltage and thus the folded cascode is a more efficient amplifier.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have provided a folded cascode amplifier to provide the input signal "V_{IN}" input therefore to allow for efficient amplification of a remote signal as is taught by Sedra and as common knowledge in the art.

The Dowlatabdi reference is silent on the composition of the operational sense amplifiers like 28 and 29.

Germano discloses a common art recognized equivalent form of operational amplifier.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used a transconductance operational amplifier because as the Dowlatabdi reference is silent on the exact structure of the operational sense amplifier used one of ordinary skill in the art would have been motivated to use any art-recognized equivalent operational amplifier such as the transconductance operational amplifier as disclosed by Germano.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant should make note that many of the claims are just so broad that references that include the US 6,836,150 Patent and the US 6,320,422 reads on these claims. In particular applicant should note elements like 202 and 206 in the '422 Patent and Figure 2 of the '150 Patent. In the interest of being concise these rejection, but the examiner has made applicant aware of this prior art should applicant decide to amend the claims and hopefully this would helpful to applicant in drafting amendments if applicant decides to amend the claims to overcome the rejection made above.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. Shingleton whose telephone number is (571) 272-1770.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal, can be reached on (571)272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MBS
December 21, 2006

Michael B Shingleton
Michael B Shingleton
Primary Examiner
Group Art Unit 2817